Device Description

NDCM 500-HMI

netX DIMM Module

Edition: 2
Language: English (EN)

Hilscher Gesellschaft für Systemautomation mbH

Web: www.hilscher.com

List of Revisions

Index	Date	Version	Chapter	Revisions
1	09.05.06	1	all	Created
1	14.12.06	1	all	Revised, JL
2	25.05.07	1	2.2 5	Added information about the system connector Technical data fieldbus: CAN, DeviceNet, PROFIBUS

Although this device has been developed with great care and was intensively tested, Hilscher Gesellschaft für Systemautomation mbH cannot guarantee the suitability of this device for any purpose not confirmed by us in writing.

Guarantee claims shall be limited to the right to require rectification. Liability for any damages which may have arisen from the use of this device or its documentation shall be limited to cases of intent.

We reserve the right to modify our products and their specifications at any time in as far as this contribute to technical progress. The version of the manual supplied with the device applies.

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1 Description

1.1 Introduction

The netX DIMM Module is a CPU module in the well known DIMM form factor, featuring a netX communication controller, which allows quick and easy implementation of Real Time Ethernet communication and standard fieldbus interfaces.

Being a complete and already fully tested CPU system, integrating Flash- and RAM memory, crystals, reset generator and DC/DC converter, the NDCM500-HMI frees the hardware designer from all the common obstacles that usually come with an own CPU hardware design, allowing the use of simple (down to 2 Layer PCBs, depending on application) custom application boards (baseboards) that usually only host the required connectors and physical interfaces for Ethernet and fieldbus interfaces, hence reducing design and product cost and time-to-market.

Along with Windows CE or Linux operating systems (appropriate board support packages are available) the NDCM 500-HMI module provides soft-keys (Touchpanel), Compact Flash (additional external components required) or SD/MMC-Card and USB interface, making it an excellent solution for the design of machine terminals.

The NDCM500-HMI is also available with PCI Bus Interface, which however is subject to certain application restrictions and licensing regulations. Please contact the Hilscher sales department for any details.

For evaluation purposes, a starter board is available, providing a connector to host the netDIMM Module. The netDIMM Starter Board comes with interfaces for Ethernet, PROFIBUS and DeviceNet and has RS232C, USB and JTAG connectors on-board. The extension bus of the DIMM Module is available through headers for ribbon cables.

The Starter Board comes with a power supply. All together, the Starter Board has everything needed to start developing and debugging own application software, including a TFT display and a SD/MMC-Card connector.

NOTICE

Device Destruction!

- Though the NDCM100-NET has the same form factor as a DIMM-PC™, it is **neither** pin compatible to the DIMM-PC™ standard, **nor** may it be powered by a 5V power supply! The NDCM500-HMI may only be powered by a **3.3 V** power supply. Using the NDCM500-HMI in any application board designed for DIMM-PC™s or the use of a higher supply voltage than 3.3V may result in severe damage to the module! Further, all signal pins require 3.3 V signaling voltage and are **not** 5V tolerant!

DIMM-PC™ is a registered trademark of Kontron AG

1.2 Overview NDCM 500-HMI

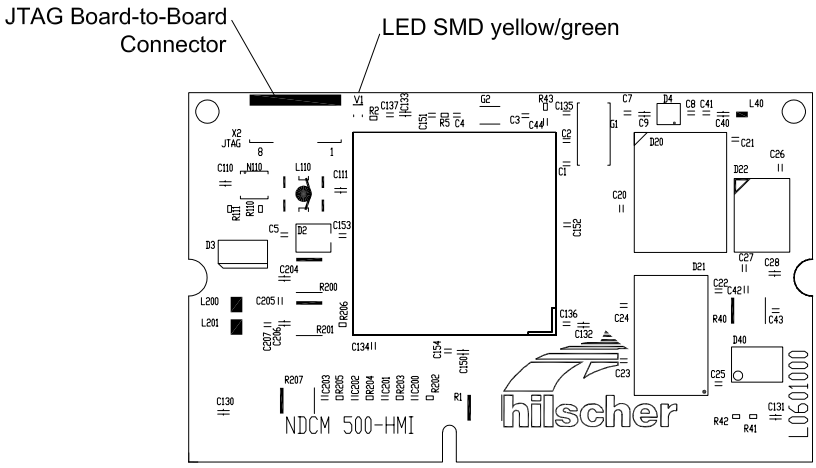


Figure 1: Overview NDCM 500-HMI

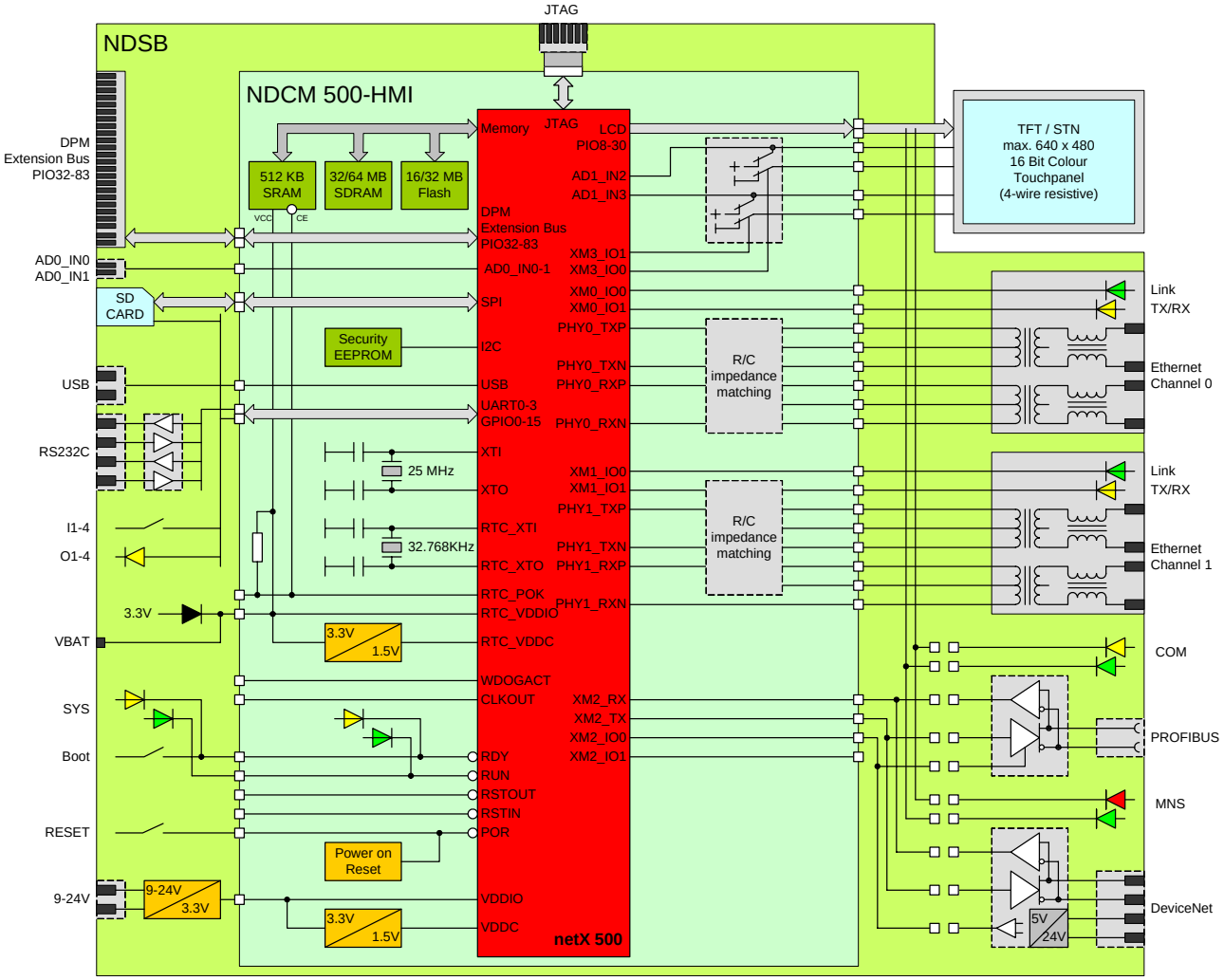


Figure 2: Block Diagram netDIMM NDCM 500-HMI and netDIMM Starter Board NDSB-HMI or NDSB-NET

The block diagram shows the netDIMM Module together with the starter board.

2 Connectors

2.1 JTAG Board-to-Board-Connector

The NDCM modules provide their JTAG Interface through an 8 pin flex cable connector (X2), located near the upper left corner of the module.

NOTE: when inserting the flex cable, the contact sides of the cable must face the printed circuit board (connector has bottom contacts)!

Pin	JTAG Signals	netX Signals
1	+3.3V	+3.3V
2	GND	GND
3	TCLK	JT_TCLK
4	TDO	JT_TDO
5	TDI	JT_TDI
6	TMS	JT_TMS
7	TRSTN	JT_TRSTN
8	GND	GND

Table 1: JTAG connector, X2

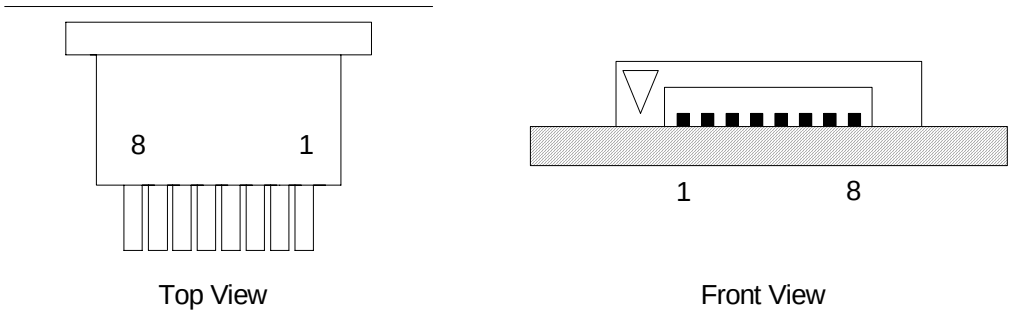


Figure 3: JTAG connector, X2

2.2 netDIMM Pinning NDCM 500-HMI

Pin	General	Ext. Bus	Prog. I/O	DPM
1	+3V3			
2	GND			
3	LCD_D00 / ETM_PSTAT0		PIO08	
4	LCD_D01 / ETM_TPKT08		PIO09	
5	LCD_D02 / ETM_TPKT09		PIO10	
6	LCD_D03 / ETM_PSTAT2		PIO11	
7	LCD_D04 / ETM_PSTAT1		PIO12	
8	LCD_D05 / ETM_TPKT11		PIO13	
9	LCD_D06 / ETM_TPKT10		PIO14	
10	LCD_D07 / ETM_TPKT12		PIO15	
11	LCD_D08 / ETM_TPKT00		PIO16	
12	LCD_D09 / ETM_TPKT01		PIO17	
13	LCD_D10 / ETM_TSYNC		PIO18	
14	LCD_D11 / ETM_TPKT13		PIO19	
15	LCD_D12 / ETM_TPKT14		PIO20	
16	LCD_D13 / ETM_TPKT02		PIO21	
17	LCD_D14 / ETM_TPKT03		PIO22	
18	LCD_D15 / ETM_TPKT05		PIO23	
19	LCD_D16 / ETM_DREQ		PIO24	
20	LCD_D17 / ETM_TPKT15		PIO25	
21	UART0_RXD		GPIO00	
22	UART0_TXD		GPIO01	
23	UART0_CTS		GPIO02	
24	UART0_RTS		GPIO03	
25	UART1_RXD		GPIO04	
26	UART1_TXD		GPIO05	
27	UART1_CTS		GPIO06	
28	UART1_RTS		GPIO07	
29	UART2_RXD		GPIO08	
30	UART2_TXD		GPIO09	
31	UART2_CTS		GPIO10	
32	UART2_RTS		GPIO11	
33			GPIO12	
34			GPIO13	
35			GPIO14	
36	IRQ		GPIO15	
37	XM2_IO1			
38	XM2_IO0			
39	XM2_RX			
40	XM2_TX			
41	XM1_IO1			
42	PHY1_RXN			
43	XM1_IO0			

Continued on next page.

Pin	General	Ext. Bus	Prog. I/O	DPM
44	PHY1_RXP			
45	XM0_IO1			
46	PHY1_TXN			
47	XM0_IO0			
48	PHY1_TXP			
49	PHY1_RXTAP			
50	PHY0_RXN			
51	PHY1_TXTAP			
52	PHY0_RXP			
53	PHY0_RXTAP			
54	PHY0_TXN			
55	PHY0_TXTAP			
56	PHY0_TXP			
57	USB_DPOS			
58	USB_DNEG			
59	+3V3			
60	GND			
61	+3V3			
62	GND			
63		CLKOUT / TCLK		
64	RDY			
65	RSTINn			
66	RUN			
67	RSTOUTn			
68	PF / RTC_POK			
69	PORn			
70	WDGACT			
71		EXT_ALE	PIO35	
72			PIO36	
73		EXT_BHEn	PIO43	DPM_BHEn
74		EXT_WRHn	PIO44	DPM_WRHn
75		EXT_WRLn	PIO45	DPM_WRLn
76		EXT_RDn	PIO52	DPM_RDn
77		EXT_RDY	PIO46	DPM_RDY
78		EXT_IRQ	PIO47	DPM_INT
79		EXT_CS0n	PIO51	DPM_CSn
80		EXT_CS1n	PIO80	*SEL_A17*
81		EXT_CS2n	PIO79	*SEL_A16*
82		EXT_CS3n	PIO84	*SEL_A18*
83		EXT_A00	PIO73	DPM_A00
84		EXT_A01	PIO70	DPM_A01

Continued on next page.

Pin	General	Ext. Bus	Prog. I/O	DPM
85		EXT_A02	PIO69	DPM_A02
86		EXT_A03	PIO66	DPM_A03
87		EXT_A04	PIO65	DPM_A04
88		EXT_A05	PIO64	DPM_A05
89		EXT_A06	PIO61	DPM_A06
90		EXT_A07	PIO60	DPM_A07
91		EXT_A08	PIO57	DPM_A08
92		EXT_A09	PIO56	DPM_A09
93		EXT_A10	PIO53	DPM_A10
94		EXT_A11	PIO50	DPM_A11
95		EXT_A12	PIO49	DPM_A12
96		EXT_A13	PIO48	DPM_A13
97		EXT_A14	PIO54	DPM_A14
98		EXT_A15	PIO55	DPM_A15
99		EXT_A16	PIO58	*(DPM_A16)*
100		EXT_A17	PIO59	*(DPM_A17)*
101		EXT_A18	PIO62	*(DPM_A18)*
102		EXT_A19	PIO63	*(DPM_A19)*
103		EXT_A20	PIO67	*SEL_A12*
104		EXT_A21	PIO68	*SEL_A13*
105		EXT_A22	PIO71	*SEL_A14*
106		EXT_A23	PIO72	*SEL_A15*
107		EXT_A24	PIO40	*SEL_A19*
108		EXT_D00	PIO83	DPM_D00
109		EXT_D01	PIO82	DPM_D01
110		EXT_D02	PIO81	DPM_D02
111		EXT_D03	PIO78	DPM_D03
112		EXT_D04	PIO77	DPM_D04
113		EXT_D05	PIO76	DPM_D05
114		EXT_D06	PIO75	DPM_D06
115		EXT_D07	PIO74	DPM_D07
116		EXT_D08	PIO32	DPM_D08
117		EXT_D09	PIO34	DPM_D09
118		EXT_D10	PIO33	DPM_D10
119		EXT_D11	PIO39	DPM_D11
120		EXT_D12	PIO38	DPM_D12
121		EXT_D13	PIO37	DPM_D13
122		EXT_D14	PIO42	DPM_D14
123		EXT_D15	PIO41	DPM_D15
124	SPI_CLK			
125	SPI_MISO			
126	SPI_MOSI			

Continued on next page.

Pin	General	Ext. Bus	Prog. I/O	DPM
127	SPI_CS0n			
128	SPI_CS1n			
129	LCD_FP / ETM_DACK		PIO27	
130	LCD_LP / ETM_TPKT04		PIO26	
131	LCD_PWR / ETM_TPKT06		PIO30	
132	LCD_CP / ETM_TPKT07		PIO29	
133	LCD_AC / ETM_TCLK		PIO28	
134	TP_YD			
135	TP_XL			
136	TP_YU			
137	TP_XR			
138	ADC0_IN0			
139	ADC0_IN1			
140	ADC0_VDDIO			
141	ADC0_VREFP			
142	ADC0_VSS			
143	+3V3BATT			
144	GND			

Table 2: netDIMM Pinning NDCM 500-HMI

Information about the connector:

On the starter board NDSB-NET the connector Molex 54698-7001 is used to connect the NDCM 100-NET.

3 Signal Description NDCM 500-HMI

Most signals of the NDCM 500-HMI are directly connected to corresponding pins of the netX chip. For any signal details, not covered by this signal description, please consult the *netX Product Brief* and the *netDIMM Design Guide*.

3.1 Power

GND

All Ground Pins of the module shall be connected to the ground plane of the baseboard.

+3V3

All +3V3 Pins of the module shall be connected to the +3.3V power plane of the baseboard.

+3V3BATT

This (optional) pin can be used to power (usually by a Lithium battery) the Real Time Clock of the netX and the module SRAM when the +3V3 power supply of the module is turned off.

3.2 General Signals

PORn

This is an active low bidirectional reset signal that can be used to automatically reset circuitry on the base/applicationboard during power up or brown-out situations. It can also be used to apply a power on reset to the NDCM 500-HMI (for example reset button on baseboard). When using this signal as an input to the NDCM 500-HMI, please note that the source for this signal must be an open collector or open drain output in order to avoid collision with the onboard reset generator of the module.

Further, as this signal is routed directly to the netX PORn input and does not trigger the onboard reset generator of the module, developers must take care, that the provided reset signal is “clean” (bounce free) and complies with the netX reset signal specifications (duration) as stated in the *netX Technical Reference Guide*.

RDY

This bidirectional signal can either be used to output netX status information or to select certain netX boot modes (together with the RUN signal). It is connected to the netX RDY pin, parallel to the yellow LED of a dual LED located on the module.

RUN

This bidirectional signal can either be used to output netX status information or to select certain netX boot modes (together with the RDY signal). It is connected to the netX RUN pin, parallel to the green LED of a dual LED located on the module.

For details on the available netX boot modes see the *netDIMM Design Guide*.

PFn / RTC_POK

This (optional) input signal comes in when the netX Powerfail functions are to be used (saving vital data to the internal Backup RAM). It is usually connected to a power fail or low voltage detection circuit at the systems power input, that can indicate a power fial condition before the power suplly actually goes down.

When not used, this signal can be left open, as the module provides a 10k pullup resistor, pulling this signal to its inactive state.

WDACT

Active high output signal of the netX Watchdog unit.

3.3 Hostinterface signals

These signals can either be inputs, outputs, bidirectional signals or PIOs, depending on the module firmware. Although Hostinterface signals on the netX basically **can** be made 5V tolerant (by powering the appropriate power pin with 5V), they are **fixed** to **3.3V** signalling voltage on the NDCM 500-HMI!

When operating in Hostinterface mode (DPM or Extension Bus) any unused signals (e.g. certain address lines) can individually be set to PIO mode and used as PIOs.

DPM_D[15:0] / EXT_D[15:0] / PIOs

Data inputs (external write) and outputs (external read) in DPM mode or data outputs (netX write) and inputs (netX read) in Extension Bus mode or PIOs.

DPM_A[19:0], SEL_A[19:12] / EXT_D[24:0] / PIOs

Address signals (inputs in DPM mode and outputs in Extension Bus mode) or PIOs. As the netX virtual DPM size is 64k, only address lines DPM_A15 to DPM_A0 are used for addressing the DPM, however instead of using the DPM_CS signal, address lines DPM_A19 to DPM_A16 (or to DPM_A15,14,13 or 12 if less than 64k is used) can be used to generate an internal DPM chip select signal by comparing these address lines either to a programmable register value or to signals applied to the SEL_A19 to SEL_A12 lines (possible application is a DIP Switch connected to the SEL_Ax lines for base address selection (-> ISA Bus))

AEN / EXT_ALE / PIO35

AEN signal (-> ISA Bus) in DPM mode or Adress Latch Enable signal in Extension Bus mode or PIO.

DPM_BHEn / EXT_BHEn / PIO43

Byte High Enable, active low (indicates access to upper Byte). Input in DPM mode, output in Extension Bus mode or PIO.

DPM_WRLn / EXT_WRLn / PIO45

Write Low Byte, active low (indicates write access to low or both bytes, depending on Firmware). Input in DPM mode, output in Extension Bus mode or PIO.

DPM_WRHn / EXT_WRHn / PIO44

Write High Byte, active low (indicates write access to upper byte). Input in DPM mode, output in Extension Bus mode or PIO.

DPM_RDn / EXT_RDn / PIO52

Read signal, active low. Input in DPM mode, output in Extension Bus mode or PIO.

DPM_RDY / EXT_RDY / PIO46

Ready or Wait signal, function and polarity programmable. Output in DPM mode, input in Extension Bus mode or PIO.

DPM_CSn / EXT_CS0n / PIO51

Chip Select Signal, active low. Input in DPM mode, output in Extension Bus mode or PIO.

EXT_CS1n / PIO80

Chip Select Signal, active low

(active within Extension Bus memory window 1) or PIO.

EXT_CS2n / PIO79

Chip Select Signal, active low

(active within Extension Bus memory window 2) or PIO.

EXT_CS3n / PIO84

Chip Select Signal, active low

(active within Extension Bus memory window 3) or PIO.

DPM_INT / EXT_IRQ / PIO47

Interrupt signal, polarity programmable. Output in DPM mode, input in Extension Bus mode or PIO.

CLOCKOUT

Clock signal output, frequency programmable.

RSTOUTn

Reset signal output, programmable.

PIO36

PIO.

3.4 Standard interface signals

3.4.1 SPI Interface

SPI_CLK

Clock signal of the SPI Interface.

SPI_MISO

Master In Slave Out. SPI Data input signal from external SPI Devices.

SPI_MOSI

Master Out Slave In. SPI Data output signal to external SPI Devices.

SPI_CS0n

SPI chip select signal 0. Output, active low.

SPI_CS1n

SPI chip select signal 1. Output, active low.

3.4.2 USB Interface

USB_DPOS

USB+ differential signal of the netX USB Interface.

USB_DNEG

USB- differential signal of the netX USB Interface. The USB signals are directly connected to appropriate netX interface pins without any further circuitry. All pullups / pulldowns and ESD protection are to be provided by the baseboard.

3.4.3 UARTs / GPIOs

UARTs and GPIOs share the same pins, while the functionality of each pin (UART or GPIO) is programmable individually. GPIO functions include PWM and interrupt functions. All UART signals are logic level signals (3.3V) and require RS-232 transceivers on the baseboard if standard serial ports are to be realized.

UART0_RXD / GPIO 0

Receive Data signal of UART0 (input) or GPIO.

UART0_TXD / GPIO 1

Transmit Data signal of UART0 (output) or GPIO.

UART0_CTS / GPIO 2

Clear To Send signal of UART0 (input) or GPIO.

UART0_RTS / GPIO 3

Request To Send signal of UART0 (output) or GPIO.

UART1_RXD / GPIO 4

Receive Data signal of UART1 (input) or GPIO.

UART1_TXD / GPIO 5

Transmit Data signal of UART1 (output) or GPIO.

UART1_CTS / GPIO 6

Clear To Send signal of UART1 (input) or GPIO.

UART1_RTS / GPIO 7

Request To Send signal of UART1 (output) or GPIO.

UART2_RXD / GPIO 8

Receive Data signal of UART2 (input) or GPIO.

UART2_TXD / GPIO 9

Transmit Data signal of UART2 (output) or GPIO.

UART2_CTS / GPIO 10

Clear To Send signal of UART2 (input) or GPIO.

UART2_RTS / GPIO 11

Request To Send signal of UART2 (output) or GPIO.

GPIO [15:12]

GPIOs.

3.5 Ethernet Signals

The module already contains all necessary pullpup / pulldown resistors and capacitors for the chip side of the Ethernet Interface. The baseboard only has to provide appropriate Transformers (see netDIMM Design Guide for details).

PHY0_RXN

Neg. differential Receive signal of Ethernet Channel 0.

PHY0_RXP

Pos. differential Receive signal of Ethernet Channel 0.

PHY0_RXTAP

Connects to the center tap of the Ethernet Transformers Receive winding for Channel 0 (Transformer is located on the baseboard).

PHY0_TXN

Neg. differential Transmit signal of Ethernet Channel 0.

PHY0_TXP

Pos. differential Transmit signal of Ethernet Channel 0.

PHY0_TXTAP

Connects to the center tap of the Ethernet Transformers Transmit winding for Channel 0 (Transformer is located on the baseboard).

PHY1_RXN

Neg. differential Receive signal of Ethernet Channel 1.

PHY1_RXP

Pos. differential Receive signal of Ethernet Channel 1.

PHY1_RXTAP

Connects to the center tap of the Ethernet Transformers Receive winding for Channel 1 (Transformer is located on the baseboard).

PHY1_TXN

Neg. differential Transmit signal of Ethernet Channel 1.

PHY1_TXP

Pos. differential Transmit signal of Ethernet Channel 1.

PHY0_TXTAP

Connects to the center tap of the Ethernet Transformers Transmit winding for Channel 0 (Transformer is located on the baseboard).

3.6 XMAC Signals (Fieldbus)

XM2_RX

Receive Data signal of XMAC2 Channel.

XM2_TX

Transmit Data signal of XMAC2 Channel.

XM2_IO0

I/O signal 0 of XMAC2 Channel.

XM2_IO1

I/O signal 1 of XMAC2 Channel.

XM0_IO0

I/O signal 0 of XMAC0 Channel.

XM0_IO1

I/O signal 1 of XMAC0 Channel.

XM1_IO0

I/O signal 0 of XMAC1 Channel.

XM1_IO1

I/O signal 1 of XMAC1 Channel.

3.7 LCD and Touchpanel Signals

These signals can either be LCD signals, ETM signals or PIOs, depending on the module firmware.

LCD_D[17:0] / ETM / PIO[25:8]

Data signals for LC Display or ETM signals or PIOs.

LCD_FP / ETM_DACK / PIO27

Frame Pulse (STN) / Vertical Pulse signal (TFT) or ETM_DACK or PIO.

LCD_LP / ETM_TPKT04 / PIO26

Line Pulse (STN) / Horizontal Pulse (TFT) signal or ETM_TPKT04 or PIO.

LCD_CP / ETM_TPKT07 / PIO29

Panel clock signal or ETM_TPKT07 or PIO.

LCD_AC / ETM_TCLK / PIO28

AC / DE signal (STN: AC bias drive, TFT : data enable output)
or ETM_TCLK or PIO.

LCD_POWER / ETM_TPKT06 / PIO30

Power Enable signal or ETM_TPKT06 or PIO.

3.7.1 Touchpanel

The NDCM500-HMI supports 4 wire resistive Touchpanels.

TP_YD

Connects to lower terminal of Touchpanel.

TP_YU

Connects to upper terminal of Touchpanel.

TP_XL

Connects to left terminal of Touchpanel.

TP_XR

Connects to right terminal of Touchpanel.

3.8 AD Converter Signals

ADC0_IN0

Analog input for ADC 0, Channel 0

ADC0_IN1

Analog input for ADC 0, Channel 1

ADC0_VDDIO

+3.3V ADC supply voltage (filtered). Can be used to power additional analog circuits (max. 150mA) on the baseboard. ***Do not connect a power source to this signal!***

ADC0_VREFP

ADC reference voltage (connected to ADC0_VDDIO through 10k serial resistor). Can be used as reference for additional analog circuits on the baseboard or to apply a different reference voltage supplied by an external source.

ADC0_VSS

Analog Ground.

4 Indicators

The NDCM 500-HMI provides an onboard Dual LED (yellow / green) for status display purposes. This LED can be driven by the RDY and RUN signals which are also routed to the modules edge connector (see also 2.3.2. General Signals).

LED	Color	State	Indicates
SYS	yellow	Flashing cyclic with 1Hz	Device is in bootstraploader mode and waiting for firmware download
	yellow	On / Off	Device may have detected monitor connection through serial or USB
	yellow		Once a firmware is loaded, it has complete control over the SYS LED states. Hence, the functionality of the SYS LEDs is application/firmware specific.
	green		

Tabelle 1: Module States LED V1

5 Technical Data NDCM 500-HMI

Technical data hardware

Parameter	Value / Range
Processor	netX 500 with 200 MHz ARM926EJ-S
Memory	16/32 MByte Flash, 32/64 MByte SDRAM, 512 Kbyte SRAM, buffered externally
LCD-Controller	up to 640x480, 16-Bit Color TFT/STN, Touchpanel Interface (4 wire resistive)
Standard Interfaces	USB 1.1, SPI, 3x UART or 16x GPIO, JTAG
AD-Converter	2 Channels (multiplexed), 10-Bit,1MS/s, S&H
2 Ethernet-Ports	10BASE-T/100BASE-TX, integrated PHYs
Hostinterface	Dual-Port Memory up to 64 KByte or Extension Bus or 52 x IO
Power Supply	+3,3 V ±5 % / 750 mA
Dimensions (L x W x T)	67.6 x 40 x 9.5 mm (including heat sink) (mechanically complies with DIMM Standard)
Operating Temperature	-25 °C ... 65 °C

Table 3: Technical Data NDCM 500-HMI

Special features for communication protocols

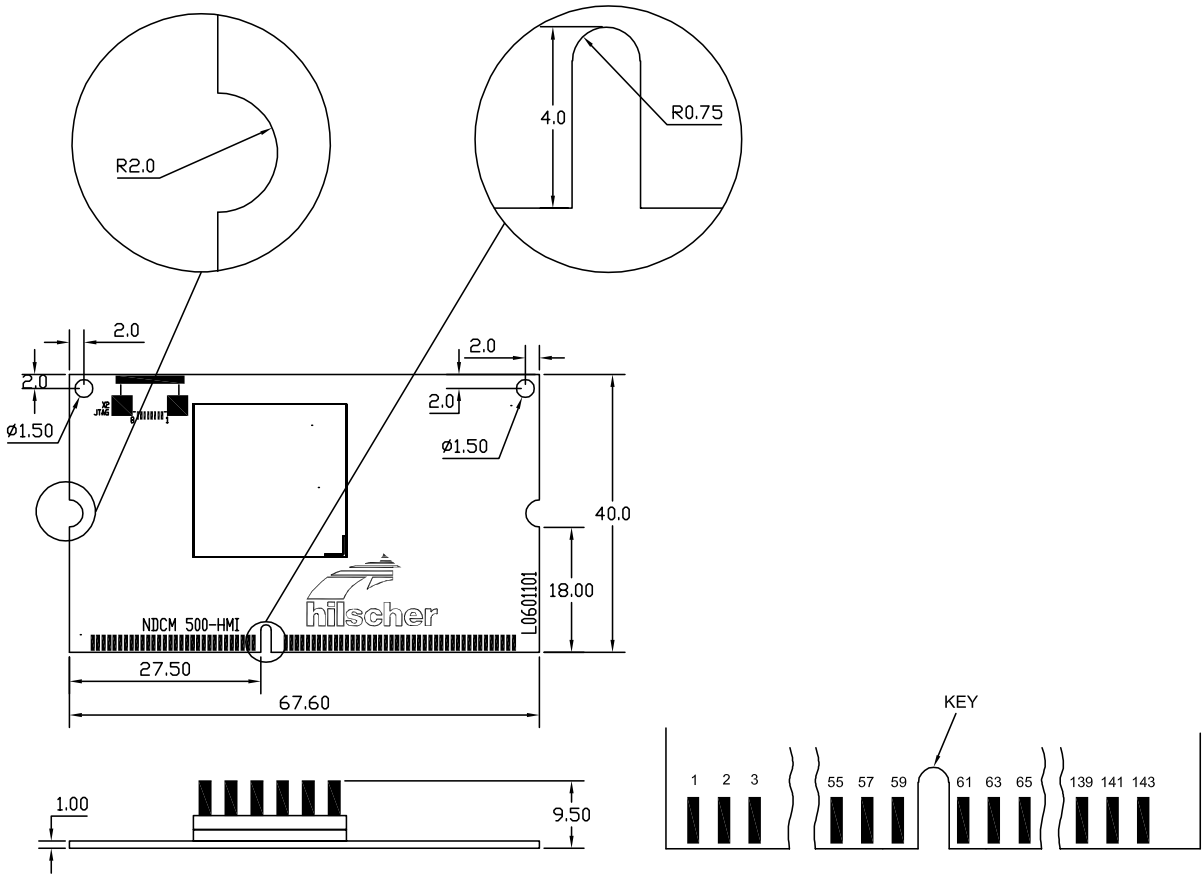
Parameter	Value / Range
2 Ethernet-Ports	IEEE 1588 EtherCAT with 3 FMMUs and 4 SyncManager EtherNet/IP Powerlink, integrated Hub, Response Delay max.1µs PROFINET, integrated Switch SERCOS III
Fieldbus Controller	CAN, DeviceNet, PROFIBUS

Table 4: Basic Technical Data for communication protocols NDCM 500-HMI

The special features are only usable with the corresponding protocol stack.

6 Mechanical Dimensions

- all dimensions in mm -



7 Lists

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