



HAL
Overview
netX 5/10/50/100/500

Hilscher Gesellschaft für Systemautomation mbH

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1 Introduction

1.1 About this Document

This manual describes the function of a Hardware Abstraction Layer (HAL) and gives an overview about available Hardware Abstraction Layers based on netX technology. This overview also includes features and limitations of each Layer1/2 interface.

1.2 List of Revisions

Rev	Date	Name	Chapter	Revisions
1	19.10.07	AO		Created Updated with Ethernet Powerlink Controlled Node, PROFINET IRT, AS-Interface Master, CC-Link Slave
2	06.05.08	HPf		Added SPI Slave
3	16.05.08	HPf		Updated availability list for netx50
4	05.06.08	AO		Added MVB device, PROFIBUS Master/Slave
5	25.07.08	AO		Added SPI Master
6	28.07.08	AO		Added Version information for each HAL Included CAN HAL timestamp functionality
7	23.01.09	AO		Added column in overview Added VARAN client Added CompoNet slave
8	06.02.09	HPf		Updated XC_UART
9	24.03.09	AO		Inserted netX10, changed docu style
10	29.04.10	AO		Updated EtherCAT features Changed docu format to current Hilscher style
11	07.06.10	AO		added CompoNet Slave for netX 5 updated CompoNet technical features
12	09.07.10	HPf		added EtherNet/IP DLR
13	2010-10-14	AO		added HALs for netX10
14	2011-01-06	AO		Added PROFIBUS Slave HAL Updated PROFIBUS FDL HAL Features and Limitations

Table 1: List of Revisions

1.3 Terms, Abbreviations and Definitions

Term	Description
MAC	Media Access Controller
HAL	Hardware Abstraction Layer
QoS	Quality of Service
VLAN	Virtual Local Area Network
xMAC	flexible Media Access Controller
xPEC	flexible Protocol Execution Controller
UART	Universal Asynchronous Receiver Transmitter
CAN	Controller Area Network
SSI	Serial Synchronous Interface
SPI	Serial Peripheral Interface
MVB	Multi Vehicle Bus
CN	Controlled Node (Slave in Ethernet Powerlink Networks)
PB	PROFIBUS
FDL	Fieldbus Datalink Layer
DLR	Device Level Ring Protocol

Table 2: Terms, Abbreviations and Definitions

All variables, parameters, and data used in this manual have the LSB/MSB (“Intel”) data format. This corresponds to the convention of the Microsoft C Compiler.

All IP addresses in this document have host byte order.

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2 The Interface

This section describes the function of a HAL and lists features and limitations of each HAL implementation.

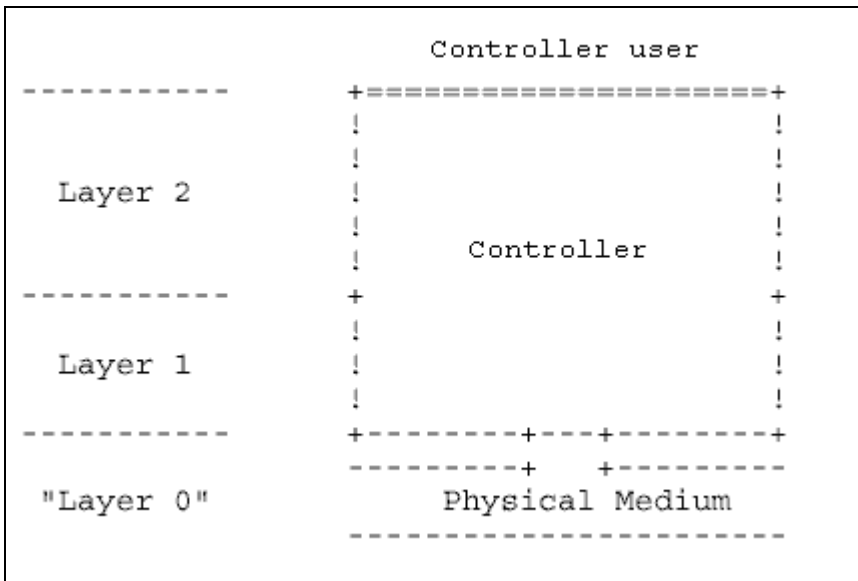


Figure 1: Interface between Interface User and Interface in Relation to Layer Model

2.1 Function

A Hardware Abstraction Layer describes the functional interface to a Controller unit. (e.g. Media Access Controller, Bus Master Controller or Bus Slave Controller). The Controller functionality is implemented using xPEC and xMAC units of netX. It is a description of how to configure the Controller and how to exchange data with the Controller in general with the aim to support and lead you during the integration process of the given Controller into your application running under your own operating system. To get a better view about interactions between the HAL user and the HAL in most of the implementations there is a small example how the HAL is used.

The xC ports numbered with port number 0, 1, 2 and 3.

2.2 Overview

Please note that details for netX500 are also suitable for netX100.

An “x” means HAL is released and available.

“-“ means that HAL is not running on netX due technical reasons.

“b” means that HAL is not released yet but in beta-phase.

Term	Number of required XC ports / Used XC ports			available				Remark
	500	5/50	10	500	50	5	10	
netX	500	5/50	10	500	50	5	10	
Ethernet Standard MAC	1/0;1	1/0;1	1/0	x	x	x	x	
Ethernet 2-Port Switch	2/01	2/01	-	x	x	x	-	
Ethernet 2-Port Hub	2/01	2/01	-	x	x	x	-	
PROFINET IRT Switch	3/013	2/01	-	b	b		-	
EtherCAT Slave	3/013	2/01	-	x	x	x	-	
POWERLINK Controlled Node	3/013	2/01	-	b	b		-	
VARAN Client	3/013	2/01	-	x	x	x	-	
SERCOS III Device	3/013	2/01	-				-	planned 2010
EtherNet/IP DLR	3/013	2/01	-	b	b		-	
PROFIBUS FDL	1/0;1;2;3	1/0;1	0/1	x	x	x	x	
PROFIBUS Slave	1/0;1;2;3	1/0;1	0/1	x	x		x	
CAN	1/0;1;2;3	1/0;1	0/1	x	x	x	x	
CC-Link Device	1/0;1;2;3	1/0;1	0/1	x	x	x	x	
CompoNet Slave	1/0;1;2;3	1/0;1	0/1	x	x	x	x	
MVB Device without redundancy / with redundancy	1/0;1;2;3 2/01;23	1/0;1 2/01	1/0 -	x	x	x	-	incl. MVB Analyzer firmware image for NXHX500-RE
AS-Interface Master	1/0;1;2;3	1/0;1	1/0	x	x			
UART Controller	1/0;1;2;3	1/0;1	1/0	x	x	x	x	
SSI Controller	1/0;1;2;3	1/0;1	1/0	x	x			
SPI Master	1/0;1;2;3	1/0;1	1/0	x				
SPI Slave	1/0;1;2;3	1/0;1	1/0	x				

Table 3: Overview of HALs

2.3 Features and Limitations

2.3.1 Ethernet Standard MAC

Technical Data

- 10BASE-T/100BASE-TX/FX operation in full/half duplex
- Integrated Dual-PHY with MDIX and Auto-Negotiation capability
- Quality of Service capable: 2 Traffic Classes (adjustable)
- Promiscuous mode (for monitoring purposes)
- Multicast pre-filtering capable
- Direct Access to PHY status information link, duplex and speed
- Number of Ethernet frame buffers: 20
- Configurable LED behavior
- possibility to suppress confirmation of processed transmission requests
- Time stamping of incoming and outgoing Ethernet Frames at MII in IEEE1588 format

Limitations

- no frame buffer management - each Ethernet frame occupies 1560 Bytes Buffer
- no Gigabit operation

2.3.2 Ethernet Switch 2-Port (Unmanaged)

Technical Data

- 2 integrated MACs, each 10BASE-T/100BASE-TX/FX operation in full/half duplex
- Integrated Dual-PHY with MDIX and Auto-Negotiation capability
- Quality of Service capable: 2 Traffic Classes (adjustable)
- Promiscuous mode (for monitoring purposes)
- Multicast pre-filtering capable
- Direct Access to PHY status information link, duplex and speed
- Number of Ethernet frame buffers: 20
- Configurable LED behavior
- possibility to suppress confirmation of processed transmission requests
- Time stamping of incoming and outgoing Ethernet Frames at MII in IEEE1588 format
- Dynamic learning based on 12-Bit hashing, aging
- Forwarding using „Store and Forward“ mechanism

Limitations

- No frame buffer management - each Ethernet frame occupies 1560 Bytes Buffer
- No Gigabit operation
- No MAC-pause mechanism in full-duplex, no back-pressure in half-duplex
- No broadcast-storm control
- No static learning

2.3.3 Ethernet Hub 2-Port

Technical Data

- 2 ports
- combined Link/Activity LED, Collision LED
- 100BASE-TX/FX operation in half duplex
- Promiscuous mode (for monitoring purposes)
- Number of Ethernet frame blocks: 40
- 2 request and 2 indication priorities (based on VLAN priority)
- Multicast pre-filtering capable
- Time stamping of incoming Ethernet Frames at MII in IEEE1588 format

Limitations

- no jabber detection and no partitioning
- no 10BASE-T operation
- no time stamping of outgoing Ethernet Frames

2.3.4 CAN Controller

Technical Data

- FullCAN Controller
- Fully Compliant with CAN Standard rev 2.0 A and rev 2.0 B
- 2 request queues (high priority, low priority)
- 2 indication queues (high priority, low priority)
- 1 confirmation queue
- Number of elements per queue is adjustable
- Single-shot mode
- Abort transmission possible
- Confirmation suppression possible
- Listen-only mode for baud rate detection and bus monitoring
- Baudrate detection with only one CAN node possible
- Different acceptance filters for Standard and Extended CAN frames
- Filtering of standard frames for each Standard identifier selectable
- Priority of standard frames for each Standard identifier selectable
- 8 Extended identifier/Rtr combinations are able to declare as high prior
- transmission and reception timestamp included in each confirmation/indication
- edge detection at xMAC IO0 and xMAC IO1 (e.g. for power-failed signal in DeviceNet)
- supported baudrates: 10/12.5/20/50/100/125/250/500/800/1000kBaud
- all CAN frame content except stuff bits are indicated to user to allow CRC recalculation

Limitations

- No TTCAN (Time Triggered CAN) functionality
- bit timing parameters (PhaseSeg1, PhaseSeg2, IPT, SJW) are fixed and not adjustable

2.3.5 UART Controller

Technical Data

- Full-duplex asynchronous operation
- Baud rates from 6 Baud up to 10 MBaud
- 1 to 16 data bits
- 1 to $2^{16}-1$ stop bits
- Optional parity control
- Inversion of data bits
- Inversion of start and stop bits
- Programmable shift direction on bus (LSB first or MSB first)
- Break detection and generation
- Programmable RTS/CTS handshake or RS485 bus mode
- FIFO and block oriented operation modes
- Programmable inter-frame gap timeout

2.3.6 SSI Controller

Technical Data

- Master, slave and monitor operation mode
- Data width between 0 and 64 bit
- SSI clock frequency between 5kHz and 3.000kHz
- cable break monitoring in master mode
- clock timeout monitoring an slave Mode
- Single and multiple transfer capable
- Master: 1 request queues, 1 confirmation queue, 1 data in queue
- Slave: 1 data out queue
- Monitor: 1 indication queue

2.3.7 EtherCAT Slave Controller

Technical Data netX 100/500

- Full Slave with integrated AL
- 2 Ethernet Interfaces 100BASE-TX/FX, 1 green Link/Activity LED per Ethernet Interface
- integrated Dual-PHY (supports Autonegotiation and Autocrossover)
- 2 LEDs for EtherCAT State Machine (ESM): RUN (green) and ERROR (red)
- Number of FMMUs: 3, Number of SYNCMANs: 4
- Fixed FMMU/SM Assignment with Mailbox Support:
 - Sync Manager 0 assigned to Receive Mailbox, Size: 128 Byte
 - Sync Manager 1 assigned to Transmit Mailbox Size: 128 Byte
 - Sync Manager 2 assigned to Receive PDO Size: 0..512 Byte, optional Watchdog
 - Sync Manager 3 assigned to Transmit PDO Size: 0..512 Byte
 - FMMU 0 mapped to Receive PDO
 - FMMU 1 mapped to Transmit PDO
 - FMMU 2 mapped to Fill Status of Transmit Mailbox
- Distributed Clocks (32 Bit) with Isochronous PDI functionality (Sync0, Sync1)
- supports Synchronization Modes:
 - Freerun (Slave's application is not synchronized to EtherCAT)
 - Synchron with SYNCMAN Event (Slave's application is synchronized to the SM2/3 Event)
 - Synchron with SYNC Event (Slave's application is synchronized to the SYNC0 or SYNC1 Event)

Limitations netX 100/500

- no DC Latch Functionality
- no MIO (Phy Management Interface) access from EtherCAT Master side
- no ReadWrite commands supported (APRW, FPRW, BRW, LRW)
- the sum of Receive PDO and Transmit PDO is limited to 512 Byte

Technical Data netX 50

- Complex Slave with integrated AL
- 2 Ethernet Interfaces 100BASE-TX/FX, 1 green Link/Activity LED per Ethernet Interface
- integrated Dual-PHY (supports Autonegotiation and Autocrossover)
- 2 LEDs for EtherCAT State Machine (ESM): RUN (green) and ERROR (red)
- Number of FMMUs: 8, Number of SYNCMANs: 8
- Recommended FMMU/SM Assignment with Mailbox Support:

Sync Manager 0 assigned to Receive Mailbox,	Size: 128 Byte
Sync Manager 1 assigned to Transmit Mailbox,	Size: 128 Byte
Sync Manager 2 assigned to Receive PDO	Size: 0..1024 Byte, optional Watchdog
Sync Manager 3 assigned to Transmit PDO	Size: 0..1024 Byte
- Distributed Clocks (32 Bit) with Isochronous PDI functionality (Sync0, Sync1)
- supports Synchronization Modes:
 - Freerun (Slave's application is not synchronized to EtherCAT)
 - Synchron with SYNCMAN Event (Slave's application is synchronized to the SM2/3 Event)
 - Synchron with SYNC Event (Slave's application is synchronized to the SYNC0 or SYNC1 Event)

Limitations netX 50

- no DC Latch Functionality
- no MIO (PHY Management Interface) access from EtherCAT Master side
- physical ReadWrite commands not supported (APRW, FPRW, BRW)

Technical Data netX 5

- Complex Slave with integrated AL
- strongly recommended external PHY: Broadcom BCM5241
- 2 Ethernet Interfaces 100BASE-TX/FX, 1 green Link/Activity LED per Ethernet Interface
- 2 LEDs for EtherCAT State Machine (ESM): RUN (green) and ERROR (red)
- Number of FMMUs: 8, Number of SYNCMANs: 8
- Recommended FMMU/SM Assignment with Mailbox Support:

Sync Manager 0 assigned to Receive Mailbox,	Size: 128 Byte
Sync Manager 1 assigned to Transmit Mailbox,	Size: 128 Byte
Sync Manager 2 assigned to Receive PDO	Size: 0..1024 Byte, optional Watchdog
Sync Manager 3 assigned to Transmit PDO	Size: 0..1024 Byte
- Distributed Clocks (32 Bit) with Isochronous PDI functionality (Sync0, Sync1)
- supports Synchronization Modes:
 - Freerun (Slave's application is not synchronized to EtherCAT)
 - Synchron with SYNCMAN Event (Slave's application is synchronized to the SM2/3 Event)
 - Synchron with SYNC Event (Slave's application is synchronized to the SYNC0 or SYNC1 Event)

Limitations netX 5

- no DC Latch Functionality
- no MIO (Phy Management Interface) access from EtherCAT Master side
- physical ReadWrite commands not supported (APRW, FPRW, BRW)

2.3.8 Ethernet POWERLINK Controlled Node

Technical Data

- ETHERNET POWERLINK V2 Controlled Node
- integrated 2-Port HUB
- integrated DUAL-PHY (not netX 5)
- Filter for PollRsp, PollReq and ASnd of all Controlled Nodes within Segment (to enable cross communication and to ease the ARM)
- SoC received signal @xm3.io0 (polarity hi/lo, delayable) to trigger external HW (Host Controller, Drive, DSP, ...)
- Fast Poll Response (Response time < 2µs) sent automatically from xPEC (3-Buffer mechanism between ARM and xPEC)
- Ident Response, Status Response are sent automatically from xPEC (3-Buffer mechanism between ARM and xPEC)
- Response to "NMT Request Invite" and Response to "Unspecific invite" are sent automatically in HW to ease the ARM (req fifo high/low)
- EPL Specific Interrupts to ARM: SoC received, PReq received, PRsp sent, SoA received
- Indicators
combined Link/Activity LED per port (pin xm0/1.io0)
optional Collision LED per port (pin xm0/1.io1)
- TimeStamp of last received SoC accessible from ARM
- lots of error diagnostic counters (also EPL specific ones)
- distinction between "Basic Ethernet Mode" and "EPL Mode" is done in hardware

Limitations

- integrated hub has no Gigabit Ethernet support
- integrated hub has no jabber detection and no partitioning
- integrated hub has no 10BASE-T operation
- no multicast pre-filtering

2.3.9 CC-Link Slave

Technical Data

- Remote I/O station and Remote Device station
- Cyclic transmission and Extended cyclic transmission
- Cyclic Message transmission/ reception
- Transient Message transmission/ reception
- Easing of cable length between stations
- Number of occupied stations: 1..4
- Supported CC-Link baud rates (bps): 10M/5M/2.5M/625k/156k
- Support CC-Link version: 1.00 / 1.10 / 1.11 / 2.00

Limitations

- No Master functionality
- No Local Station functionality
- No Intelligent Device functionality

2.3.10 PROFINET IRT 2-Port Switch

Technical Data

- 2 integrated MACs, 10BASE-T/100BASE-TX/FX operation in full/half duplex
- Quality of Service capable: 2 Traffic Classes (adjustable)
- Promiscuous mode (for monitoring purposes)
- Direct access to PHY status information link, duplex and speed
- Forwarding using “Store and Forward” mechanism (green IRT interval)
- Forwarding using “Cut-Through” mechanism (red IRT interval)
- Time-stamping at MII in receive and transmit direction
- Sync-signal generation for IRT certification
- IRT phase control (red-green-yellow intervals)
- Automatic RTC3 frame handling
- Transparent-clock synchronization mechanism

Limitations

- no MAC-pause mechanism in full-duplex, no back-pressure in half-duplex
- no broadcast-storm control
- no static learning
- no frame buffer management in green interval - each Ethernet frame occupies 1560 bytes buffer

2.3.11 AS-Interface Master

Technical Data

- Applies to AS-Interface specification Version 3.0 Revision 1.
- Extended addressing capable.
- Full execution control without requirement of host CPU interaction during operation (offline, detection, activation, data exchange, inclusion and management phases).
- Provides execution control interface as specified in AS-Interface specification for most administrative functions.
- Optional high-performance mode, where input data can be processed during a still running data exchange cycle (allows fast processing of combined transaction profiles).
- Optional transparent mode, where execution control is disabled and host can send and receive commands transparently (no real-time capability).

Limitations

- Combined transactions are not part of the execution control unit but can be implemented on the host CPU.

2.3.12 SPI Slave

Technical Data

- Up to 10 MHz clock rate.
- SPI Modes 1 and 3 are supported (CPHA = 1, CPOL = 0/1).
- MSB or LSB first selectable.
- FIFO watermark supervision.

Limitations

- SPI Modes 0 and 2 (CPHA = 0) are not supported.

2.3.13 MVB device

Technical Data

- MVB device class 1 and 2
- ESD or EMD physical interface
- Up to 256 process datasets
- Triple-buffered process datasets
- Line redundancy support
- Message queues with 100 entries in total
- MVB event handling

Limitations

- no OGF physical interface

2.3.14 PROFIBUS FDL

Technical Data

- support of PROFIBUS-DP, PROFIBUS-FMS und PROFIBUS-PA
- active (Master) and passive (Slave) station functionality
- 32 KBytes communication RAM (1 internal RAM segment used)
- complete processing of Physical Layer 1 and Data link Layer 2 of the ISO/OSI Model including token handling, message transfer processing and fault detection relieving the host processor from all timing critical tasks
- Supported baud rates: 9.6, 19.2, 31.25, 45.45, 93.75, 187.5, 500 kbaud, 1.5, 3, 6, 12 Mbaud
- Autobaud detection
- Supported services: Request-FDL-Status, SDN, SDA, SRD, MSRD, CS
- suppression of GAP check due setting HSA and TS to zero
- 127 active (Master) and passive (Slave) stations, mixable
- support of 64 Service Access Points and a Default-SAP
- Clock Synchronization support: Time master support

Limitations

- No region/DL-segment addresses support
- No transmission of SD3 frames (but reception is possible)
- Unsupported service: CSRD (ignored by PROFIBUS FDL controller)
- Unsupported service: Ident with reply (ignored by PROFIBUS FDL controller)
- Unsupported service: LSAP status with reply (ignored by PROFIBUS FDL controller)
- Clock Synchronization: no Time receiver support
- No Cross communication support (Publisher/ Subscriber)
- No equidistant cycle support for isochrone applications (DPV2)

2.3.15 PROFIBUS Slave

Technical Data

- Support of PROFIBUS-DP and PROFIBUS-FMS
- Passive (Slave) station functionality
- 32 KBytes communication RAM (1 internal RAM segment used)
- Complete processing of Physical Layer 1 and Data link Layer 2 of the ISO/OSI Model including message transfer processing and fault detection relieving the host processor from all timing critical tasks
- Supported baud rates: 9.6, 19.2, 31.25, 45.45, 93.75, 187.5, 500 kbaud, 1.5, 3, 6, 12 Mbaud
- Autobaud detection
- Cross communication support (Publisher and parallel up to 8 Subscriber links)
- Support of 64 Service Access Points and a Default-SAP
- Clock Synchronization support (CS)
- Support of clock synchronization protocol (Time receiver)

Limitations

- No active (Master) station functionality
- No region/DL-segment addresses support
- No transmission of SD3 frames (but reception is possible)
- Unsupported service: CSRD (ignored by PROFIBUS Slave controller)
- Unsupported service: Ident with reply (PROFIBUS Slave controller responds with SC)
- Unsupported service: LSAP status with reply (PROFIBUS Slave controller responds with SC)

2.3.16 SPI Master

Technical Data

- supported SPI Master modes 0..3
- 8 data bits per character
- MSB first / LSB first selection
- SPI clock between 0,763..5000 kHz in 20 ns resolution
- block oriented data exchange bytes via DMA to reduce software handling for SPI Master user (size per request between 1..1024 characters)
- user transmit buffer and user receive buffer separated to re-use transmit data after data exchange
- optional Burst Delay between bytes [0.5 bit times], range: 2..255
- Chip Select (SS)
 - handled automatically by SPI Master
 - polarity adjustable
 - possibility to disable OE signal
 - pre and post data exchange delay adjustable [0.5 bit times], range: 1..255
 - Chip select pre and post delay in half SPI clock cycles
 - optional toggling of Chip Select (SS) during burst delay
- watermark confirmation interrupt after reception of a specific number of data (e.g. after each 16/32/.../1008 bytes) to give SPI Master user the possibility to process received data during reception on the fly
- possibility to abort transfers in progress

Limitations

- no data exchange over fifo
- only one Chip Select signal handled automatically
 - Note:** The SPI Master user has opportunity to handle chip selects manually in ARM software (in this case it is only possible to have one request in request fifo to progress and the SS may not be connected to any SPI Slave)
- only support of 8 data bits per character

2.3.17 VARAN Client

Technical Data

- VARAN Protocol version 1.1.1.0 based on VARAN design specification V0.59
- 2 input (memory read) areas of 128 bytes size each (Note: areas may not overlap)
- 2 output (memory write) areas of 128 bytes size each (Note: areas may not overlap)
- PLL-functionality to synchronize client application with VARAN network
- 2 Sync Out channels supported
- integrated 2-port splitter for daisy-chain topology support
- integrated EMAC for IP data exchange with client application
- VARAN client timing attributes:

tPHY_TX	=	80 ns	... max. transmit delay Ethernet PHY
tPHY_RX	=	320 ns	... max. receive delay Ethernet PHY
tSplitter	=	200 ns	... delay from signal input in MAC to signal output
tClient	=	max. 700 ns	... processing time of VARAN client (MAC)
tClient_access	=	20 ns/byte	... internal access time of VARAN client

Limitations

- EMAC always works in Promiscuous mode, no Destination address filtering support in VARAN Controller, Destination Address filtering must be done in user application
- PLL unit only supports "Slave mode" to synchronize host application with VARAN network (see VARAN design specification V0.59 for details)
- SPI single commands (optional feature) not supported

2.3.18 CompoNet Slave

Technical Data

- CompoNet Slaves: IN, Mix and OUT
- CompoNet Slaves: Bit and Word unit
- Supported baud rates: 93,75kb, 750kb, 1,5Mb, 3Mb, 4Mb
- Autobaud detection
- Supported Frames: OUT, TRG, Beacon, B_Event, A_Event, CN and IN frames
- Transmitting of A_Event Poll request
- Cancelling of a queued A_Event poll request
- Double buffer for IN data
- Double buffer for OUT data
- One transmission Buffer for EVENT data
- One reception Buffer for EVENT data
- Monitoring mode (Analyzer) for debug and maintenance purpose

2.3.19 EtherNet/IP DLR

Technical Data

- IEEE 802.3 operation.
- Cut-through switching.
- Support for Beacon-based ring node or Ring Supervisor.
- 3 QoS queues (highest priority for DLR and CIP sync frames, high and low priority queue).
- Prioritization via 802.Q/D (VLAN) and DSCP.
- Filtering of incoming unicast and multicast to host CPU.
- Preserve IEEE 802.Q VLAN Id and tag priority of ring protocol frames.
- Configure multicast address for Beacon frames to be forwarded on ring ports.
- Configure multicast address of Announce and Locate_Fault frames to be forwarded on ring ports.
- Configure multicast address hashes (including Announce, Locate_Fault, Neighbor_Check_Request/Response and Sign_On) to be forwarded only to host CPU.
- Mechanism to flag the port through which such a frame was received from ring.
- Mechanism to forward such frames from host CPU on to ring only through the port it was intended to go out.
- Mechanism to allow sending of frames (like supervisor frames) on both ports.
- Flush unicast MAC address tables on ring state transitions.
- Unicast MAC address of self is not purged when MAC address table is flushed.
- Implement of Interface Counters and Media Counters
- Remove device's own frames from network when receiving
- Implement IEEE1588 end-to-end transparent clock
- Receive and transmit time-stamping for every frame to allow support of IEEE1588 ordinary/boundary clocks
- Block TX and RX ports for link debounce

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